In the Claims:

Claim 1 (amended). A method for fabricating a double gate MOSFET, which comprises the steps of:

providing a substrate structure having a silicon substrate layer, a first insulation layer disposed on the silicon substrate layer, a first spacer layer disposed on the first insulation layer, and a semiconductor layer disposed on the first spacer layer;

patterning the semiconductor layer resulting in a semiconductor layer structure provided as a channel of the double gate MOSFET;

depositing a second spacer layer on the semiconductor layer structure and the first spacer layer;

completely embedding the semiconductor layer structure in the first and second spacer layers by patterning the first and second spacer layers;

depositing a second insulation layer on a structure formed of the first and second spacer layers;

vertically etching two depressions disposed along one direction, the two depressions dimensioned such that the semiconductor layer structure is situated completely between them, during the etching of the two depressions, the second insulation layer, the first and second spacer layers and, in each case on both sides, an edge section of the semiconductor layer structure being etched through completely in each case;

filling the depressions with an electrically conductive material;

forming a contact hole in the second insulation layer;

selectively removing the first and second spacer layers through the contact hole made in the second insulation layer;

applying third insulation layers on inner walls of a region of removed spacer layers and on surfaces of the semiconductor layer structure; and

introducing a further electrically conductive material into the region of the removed spacer layers.

Claim 10 (amended). The method according to claim 1, which comprises selectively removing the first and second spacer layers by wet-chemical etching.